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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,249	01/14/2002	Thomas Knecht	WC0088	5303

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10-047,249	Knecht et al.
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on th cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1 - 27 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7, 11-16, 18-26 is/are rejected.

☒ Claim(s) 8, 9, 10, 17, 27 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The drawing(s) filed on 4-18-2002 is/are ~~objected to by the Examiner~~ approved by the examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4 & 5

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the voltage controlled oscillator circuit being resident in an electronic component received in the first cavity must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Claim 12 is objected to because of the following informalities: Claim 12 recites that claim 1 has "the controlled-digital logic output" yet claim 1 does not appear to have such structure. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 11-15, 18-20 and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemori et al. 6,154,095 (Shigemori) in view of Hidefumi JP2000151283 (Hidefumi).

Shigemori discloses a frequency-adjustable oscillator 5 "suitable" for digital signal clock synchronization. The oscillator 5 having a crystal oscillator circuit 1, 10 for generating a driving signal and having a voltage-variable control input (See Figure 7 and in particular the voltage applied to element 19 from the D/A converter.) for adjusting a frequency of the driving signal (See column 11, lines 24-45). The crystal oscillator inherently operates in the fundamental mode, because this mode is necessary for the gain stage of the oscillator to oscillate properly. The crystal oscillator circuit including a voltage variable capacitive element 19 responsive to the control input, an AT-cut quartz resonator (See column 9, around line 23) linked to the voltage variable capacitive element as is clearly shown in Figure 7, and a gain stage 11b for energizing the quartz resonator as is also clearly shown in Figure 7. The oscillator 5 also has a

phase detector circuit 21 for generating a phase-offset signal applied to a filter 22 that produces a VCO control signal. The VCO control signal is applied to a voltage controlled oscillator circuit (VCO) 23 that generates an analog controlled-frequency signal. The oscillator 5 also includes a frequency divider circuit 24 having a pre-selected divider ratio. The frequency divider circuit 24 is linked between the VCO and the phase detector circuit 21 for generating a reduced frequency feedback signal in response to the controlled-frequency signal. The phase detector circuit 21 being responsive to the feedback signal and the driving signal such that the phase offset signal varies according to a phase difference between the feedback signal and the driving signal (See column 6, around line 64 and the entire column 1). Shigemori also discloses a double-sided package including a platform 67 that has the crystal resonator attached to one side and the semiconductor circuit attached to the other side. Note that Figure 12 of Shigemori discloses that the IC chip that contains the voltage-controlled oscillator is housed in a first cavity.

Shigemori's double-sided package does not include the claimed sidewalls extending substantially upwardly and substantially downwardly from the outer portion of the platform so as to form first and second cavities such that the first cavity receives the quartz resonator and the second cavity receives at least one electronic component. Shigemori's double-sided package being that it does not include what applicant means by cavities also does not include a cover coupled with the first cavity defining a hermetic environment for containing the quartz resonator. Shigemori also does not show the capacitive elements, the varactor and the like being formed in the second cavity by discrete elements. Shigemori's double-sided package does not include the claimed laminate substrate coupled with the second cavity. Shigemori is silent on whether or not the AT-cut crystal is tunable, however, it is well-known that such AT-cut crystals can be made tunable and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize such a structure so as to allow for the crystal to be tuned as is conventional and well-known in the art. Shigemori is silent on temperature compensation for the crystal oscillator circuit. This is a broad claim in that any form of temperature compensation can be employed. There are many well-known forms of temperature compensation employed of a crystal oscillator arrangement. These include the actual use of a heating/cooling element to control the temperature of the package. Some measure the temperature and in accordance with calibration utilizes a look-up table to correct for temperature. All these conventional well-known temperature compensation arrangements have one goal and that is to provide a correct and stable oscillating frequency. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a conventional temperature compensation arrangement in Shigemori so as to provide for a correct and stable frequency generation as is conventionally and well-known in the art.

Hidefumi shows that a double-sided package that has a center platform 8, upper and lower side walls that forms upper and lower cavities such that the upper (first) cavity receives the resonator and the lower (second) cavity that receives electronic components and a cover 6 that hermetically seals the first cavity (See Figure 1) is an equivalent structure for packaging a PLL circuit as is known in the art. Also not only does Hidefumi provide for housing of the resonator and its associated electronic component structure, Hidefumi discloses in the abstract that such makes the crystal oscillator "capable of minimizing the flat shape of a container". Hidefumi also discloses to utilize discrete elements for the capacitor elements 4 and 5 and to house these in the second cavity. As Hidefumi recognizes, this allows for the integrated chip 3 to be subject to less noise and just like using a crystal resonator outside the IC chip saves chip space the use of the capacitive elements outside the IC chip also saves chip space. The platform also forms a laminate substrate composed of "the laminating of the ceramic insulating layers 1a and 1b". This allows the conductive paths to be formed so as to connect the resonator i.e. crystal to the IC chip and discrete components.

Therefore, because these two packages for housing a crystal oscillator structure and its associated electronic components were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the double-sided package structure of Hidefumi for the double-sided package structure of Shigemori and especially because Hidefumi teaches that such a container minimizes the flat shape (It save space). The use of a single semiconductor chip having at least the gain stage, the phase detector circuit, the VCO and the frequency divider circuit received in the second cavity would be an obvious consequence of the obvious combination above (See column 8, lines 51-55 of Shigemori).

As to the use of discrete capacitive elements namely discrete varactors housed in the second cavity, it would have been obvious to one of ordinary skill in the art at the time the invention was made to house such elements in the second cavity in the invention made obvious above because, the housing of these discrete elements in the second cavity next to the IC chip saves chip space on the IC chip and it separates the IC chip from noise as taught by Hidefumi.

As to the use of a laminate substrate coupled with the second cavity, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize such a substrate in the second cavity in the invention made obvious above because, the use of such a substrate in a double-sided arrangement allows for the connection of the resonator to the IC chip and discrete components as taught by Hidefumi. Note that the platform of Hidefumi includes a laminate substrate and more than one electronic component as noted above and thus the mounting of at least one electronic component on the

second cavity side and at least one electronic electronic component on the laminate substrate is an obvious consequence of the invention made obvious above.

Claims 12-14 set forth an "Absolute Pull Range" of at least 50ppm for the nominal operating frequencies of 622.08, 644.531, 666.514 and 669.326 Megahertz. This is merely the selection of the optimum or workable range because as admitted by applicant these values are dependent upon " operating parameters" and accordingly as the selection of the operating parameters is merely the selection of the optimum or workable range which involves routine skill in the art (In re Aller, 105 USPQ 233) the selection of these operating parameters to obtain the above specifications would have been obvious to one of ordinary skill in the art at the time the invention was made. Also see In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 18-19 set forth various "footprint" sizes that include the sizes 5 millimeters by 7 millimeters and 40 square millimeters. This is merely the selection of the optimum or workable range because this is merely dependent on the size of the chips and resonator employed and Hidefumi clearly points out as noted above that one will minimize the flat shape i.e. footprint of the package and thus this selection of the operating parameters is merely the selection of the optimum or workable range which involves routine skill in the art (In re Aller, 105 USPQ 233). Accordingly, the selection of these operating parameters to obtain the above specifications would have been obvious to one of ordinary skill in the art at the time the invention was made. Also see In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemori in view of Hidefumi as applied to claims 1-7, 11-15, 18-20 and 21 above, and further in view of Gillig 5,604,468 (Gillig).

All the above reasoning as applied above against claims 1-7, 11-15, 20 and 21 and the following: Shigemori is silent on the use of a temperature compensation logic linked to a temperature sensor for generating a capacitance adjustment based upon temperature.

Gillig in column 3, around line 5, clearly recites that it is well known to provide a crystal oscillator with a "warp element" i.e. varactor or variable capacitance element and to utilize a temperature compensation logic element 22 that is responsive to a temperature sensor 24 so as to perform a capacitance adjustment on the crystal oscillator which as is commonly known stabilizes the oscillator with respect to temperature.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the combination made obvious over Shigemori and Hidefumi as noted above with a

temperature compensation logic element linked to a temperature sensor for generating a capacitance adjustment based upon temperature so as to stabilize the crystal oscillator of the combination made obvious above as taught by Gillig.

Claims 16, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigemori in view of Hidefumi as applied to claims 1-7, 11-15, 18-20 and 21 above, and further in view of Ouyang et al. 4,706,045 (Ouyang).

All the above reasoning as applied above against claims 1-7, 11-15, 20 and 21 and the following: Shigemori is silent on where or not the buffer element 35 performs a sinewave-to-logic translator circuit.

Figure 5A of Ouyang shows that it is common place to provide such a "translator" i.e. A/D converter, on the output of a VCO so as to provide a square wave, i.e. a "logic" signal, which as is known to those of routine skill can then form the basis for a clock, or other common digital use of PLL with a VCO. (See column 8, around line 46).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the output of Shigemori with a sinewave-to-logic translator circuit so as to provide for a signal that can be utilized in digital formats as taught by Ouyang.

Allowable Subject Matter

Claims 8-10, 17 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record and especially the Hidefumi reference fails to show the side "castellations" as claimed. The prior art of record and especially Hidefumi fails to disclose or suggest a differential receiver used as a "translator" circuit that generates a digital output for PECL logic. The prior art of record and especially Hidefumi fails to show the use of a buried inductor in combination with the PLL circuitry as claimed. The prior art of record and especially Hidefumi fails to disclose the use of a printed circuit board positioned to "cover" the second cavity.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Noda et al. and Laute et al. both disclose a pll in a housing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
May 22, 2003

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817